Changes to the Specification

Please replace paragraph [0007] with the following amended paragraph:

[0007] Referring to Figs. 1 ~~and 2~~ through 3, in an AND-type flash memory device, a floating gate 24 and a control gate 26 are layered on a substrate 20 including a device isolation layer 22 and a source/drain region 28 is formed at both sides of the floating gate 24 in the substrate 24. A thin tunnel oxide 23 is formed between the substrate 20 and the floating gate 24 and a gate oxide 25 is formed between the floating gate 24 and the control gate 26. Such an AND-type flash memory device embodies densification by sharing bit line contacts and source lines in a plurality of cells and suppresses the occurrence of disturb during program operation through parallel connection and the layered bit lines and source lines.

Please replace paragraph [0019] with the following amended paragraph:

Referring to Fig. 4c, the first photoresist layer ~~42~~ 46 is removed. A first sacrificial layer is deposited over the substrate 40 including the floating gate. The first sacrificial layer may be formed of nitride. Then, a first etch back process is performed without a mask to form spacers 48 on the sidewalls of the floating gate 45. The first etch back process may be performed through a dry etching and an anisotropic etching. The spacers have an open sidewall inclined gently and, therefore, a filling material is fully deposited without creating voids in a filling process of trenches.

Please replace paragraph [0024] with the following amended paragraph:

Referring to Fig. 4h, the spacers are removed through a dry etching process using phosphoric acid at a temperature higher than, for example, 70°C and, at the same time, the remaining second sacrificial layer is completely removed. As a result, a trench-type device isolation layer 52 and a floating gate with the second trench T2 are formed on the substrate 40.

Please replace paragraph [0029] with the following amended paragraph:

In some methods, the first polysilicon layer may be 300Å~2500Å thicker than the ~~first trench~~ device isolation layer and the spacers may be formed of nitride. The sacrificial layer and the oxide layer may be formed of one selected from a group consisting of TEOS (tetraethyl orthosilicate) oxides, BPSG (borophosphosilicate glass), PSG (phosphosilicate glass), and HDP (high-density plasma) oxides. The oxide layer and the sacrificial layer may be removed by a chemical mechanical polishing (CMP) process or an etch back process. The spacers and the remaining sacrificial layer may be removed by an wet etching process using phosphoric acid at a temperature higher than 70[[Å]] °C.